

In re Patent Application of
RAYNOR
Serial No. 10/645,320
Filed: AUGUST 21, 2003

In the Claims:

This listing of claims replaces all prior versions
and listing of claims in the application.

Claims 1-13 (Cancelled).

14. (currently amended) A solid state image sensor
comprising:

a substrate of a first conductivity type;
an epitaxial layer of the first conductivity type on
said substrate; and
an active pixel array in said epitaxial layer, each
pixel comprising

a first well of a second conductivity type
functioning as a collection node,

at least one second well of the first
conductivity type adjacent said first well, and

a plurality of MOS transistors of only the
second conductivity type functioning as active
elements of said pixel; and

circuit elements external said active pixel array,
said external circuit elements comprising a respective
comparator and counter for each pixel.

15. (Previously presented) A solid state image
sensor according to Claim 14, wherein the first conductivity
type comprises a P-type conductivity, and the second
conductivity type comprises an N-type conductivity.

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16. (Previously presented) A solid state image sensor according to Claim 14, wherein the first conductivity type comprises an N-type conductivity, and the second conductivity type comprises a P-type conductivity.

17. (currently amended) A solid state image sensor according to Claim 14, ~~further comprising circuit elements external said active pixel array;~~ and wherein said active elements in each pixel and said external circuit elements form part of an analog-to-digital converter.

18. (currently amended) A solid state image sensor according to Claim 17, ~~further comprising at least one comparator external said active pixel array;~~ and wherein said active elements in each pixel form an amplifier connected to said ~~at least one~~ comparator for forming part of the analog-to-digital converter.

19. (currently amended) A solid state image sensor according to Claim 18, wherein said active elements in each pixel are selectively switched to said ~~at least one~~ comparator.

20. (currently amended) A solid state image sensor according to Claim 18, wherein said circuit elements external each pixel comprise at least one current mirror connected to said ~~at least one~~ comparator; and wherein said active elements

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in each pixel form a differential amplifier for receiving a pixel photodiode voltage and a reference voltage, and for providing a balanced output to said at least one current mirror connected thereto.

21. (Previously presented) A solid state image sensor according to Claim 18, further comprising a latch connected to said at least one comparator in which a count is latched by a change of state of said at least one comparator.

22. (Previously presented) A solid state image sensor according to Claim 21, further comprising a frame store circuit connected to said latch for receiving the count latched by said latch.

23. (Previously presented) A solid state image sensor according to Claim 20, wherein the reference voltage is ramped during a time when each pixel is integrating a photo induced current.

24. (Previously presented) A solid state image sensor according to Claim 20, wherein the reference voltage is ramped during reset of each pixel to provide an offset compensation.

25. (canceled).

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26. (currently amended) A solid state image sensor
~~according to Claim 14, further comprising:~~

a substrate of a first conductivity type;

an epitaxial layer of the first conductivity type on
said substrate;

an active pixel array in said epitaxial layer, each
pixel comprising

a first well of a second conductivity type
functioning as a collection node,

at least one second well of the first
conductivity type adjacent said first well, and
a plurality of MOS transistors of only the second
conductivity type functioning as active elements of said
pixel; and

circuit elements external said active pixel array,
said external circuit elements comprising comparators and
counters, and wherein a number of pixels in a given row or
column of said active pixel array share a single comparator
and counter, with the corresponding pixels in the given row or
column being enabled sequentially.

27. (Previously presented) A solid state image
sensor according to Claim 26, wherein said active elements in
each pixel form a differential amplifier, and outputs of said
differential amplifier are multiplexed to a pair of output
lines common to the corresponding pixels in the given row or
column.

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28. (Previously presented) A solid state image sensor according to Claim 27, wherein the active elements in each pixel further comprise cascode transistors connected to the outputs of each differential amplifier.

29. (currently amended) A solid state image sensor comprising:

a substrate;

an active pixel array in said substrate, each pixel comprising

a first well of a first conductivity type functioning as a collection node,

at least one second well of a second conductivity type adjacent said first well, and

a plurality of MOS transistors of only the first conductivity type functioning as active elements; and

circuit elements in said substrate and external said active pixel array and forming analog-to-digital converters with the active elements therein, the external circuit elements further comprising a respective comparator and counter for each pixel.

30. (Previously presented) A solid state image sensor according to Claim 29, wherein said substrate is of the second conductivity type; and wherein the first conductivity type comprises a P-type conductivity and the second conductivity type comprises an N-type conductivity.

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31. (Previously presented) A solid state image sensor according to Claim 29, wherein said substrate is of the first conductivity type; and wherein the first conductivity type comprises an N-type conductivity and the second conductivity type comprises a P-type conductivity.

32. (currently amended) A solid state image sensor according to Claim 29, ~~wherein said circuit elements external each pixel comprise at least one comparator,~~ and wherein said active elements in each pixel form an amplifier connected to said ~~at least one~~ comparator for forming an analog-to-digital converter.

33. (currently amended) A solid state image sensor according to Claim 32, wherein said active elements in each pixel are selectively switched to said ~~at least one~~ comparator.

34. (Previously presented) A solid state image sensor according to Claim 32, wherein said circuit elements external each pixel comprise at least one current mirror connected to said at least one comparator; and wherein said active elements in each pixel form a differential amplifier for receiving a pixel photodiode voltage and a reference voltage, and for providing a balanced output to said at least one current mirror connected thereto.

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35. (currently amended) A solid state image sensor according to Claim 32, further comprising a latch connected to said ~~at least one~~ comparator in which a count is latched by a change of state of said at least one comparator.

36. (Previously presented) A solid state image sensor according to Claim 35, further comprising a frame store circuit connected to said latch for receiving the count latched by said latch.

37. (Previously presented) A solid state image sensor according to Claim 34, wherein the reference voltage is ramped during a time when each pixel is integrating a photo induced current.

38. (Previously presented) A solid state image sensor according to Claim 34, wherein the reference voltage is ramped during reset of each pixel to provide an offset compensation.

39. (canceled).

40. (Previously presented) A solid state image sensor ~~according to Claim 29,~~ comprising:
a substrate;
an active pixel array in said substrate, each pixel
comprising

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a first well of a first conductivity type
functioning as a collection node,
at least one second well of a second
conductivity type adjacent said first well, and
a plurality of MOS transistors of only the
first conductivity type functioning as active
elements; and
circuit elements in said substrate and external said
active pixel array and forming analog-to-digital converters
with the active elements therein;

wherein said circuit elements external each pixel
further comprise comparators and counters for said active
pixel array, and wherein a number of pixels in a given row or
column of said active pixel array share a single comparator
and counter, with the pixels being enabled sequentially.

41. (Previously presented) A solid state image
sensor according to Claim 40, wherein said active elements in
each pixel form a differential amplifier, and outputs of said
differential amplifier are multiplexed to a pair of output
lines common to the corresponding pixels in the given row or
column.

42. (Previously presented) A solid state image
sensor according to Claim 41, wherein the active elements in
each pixel further comprise cascode transistors connected to
the outputs of each differential amplifier.

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43. (currently amended) A method for making a solid state image sensor comprising:

forming an active pixel array in a substrate, and
forming each pixel comprising

forming a first well of a first conductivity type functioning as a collection node,

forming at least one second well of a second conductivity type adjacent the first well,

forming a plurality of MOS transistors of only the first conductivity type functioning as active elements; and

forming circuit elements in the substrate external the active pixel array and forming analog-to-digital converters with the active elements therein;

wherein the circuit elements external each pixel further comprise a respective comparator and counter for each pixel.

44. (currently amended) A method according to Claim 43, ~~wherein the circuit elements external each pixel comprise at least one comparator, and~~ wherein the active elements in each pixel form an amplifier connected to the at least one comparator for forming an analog-to-digital converter.

45. (currently amended) A method according to Claim 44, wherein the active elements in each pixel are selectively switched to the ~~at least one~~ comparator.

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46. (currently amended) A method according to Claim 44, wherein the circuit elements external each pixel comprise at least one current mirror connected to the ~~at least one~~ comparator; and wherein the active elements in each pixel form a differential amplifier for receiving a pixel photodiode voltage and a reference voltage, and for providing a balanced output to the at least one current mirror connected thereto.

47. (currently amended) A method according to Claim 44, further comprising a latch connected to the ~~at least one~~ comparator in which a count is latched by a change of state of the ~~at least one~~ comparator.

48. (Previously presented) A method according to Claim 47, further comprising a frame store circuit connected to the latch for receiving the count latched by the latch.

49. (canceled).

50. (Previously presented) A method ~~according to Claim 43~~, for making a solid state image sensor comprising:
forming an active pixel array in a substrate, and
forming each pixel comprising
forming a first well of a first conductivity
type functioning as a collection node,
forming at least one second well of a second
conductivity type adjacent the first well,

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forming a plurality of MOS transistors of
only the first conductivity type functioning as
active elements; and
forming circuit elements in the substrate external
the active pixel array and forming analog-to-digital
converters with the active elements therein, wherein the
circuit elements external each pixel further comprise
comparators and counters for the active pixel array, and
wherein a number of pixels in a given row or column of the
active pixel array share a single comparator and counter, with
the pixels being enabled sequentially.

51. (Previously presented) A method according to
Claim 50, wherein the active elements in each pixel form a
differential amplifier, and outputs of the differential
amplifier are multiplexed to a pair of output lines common to
the corresponding pixels in the given row or column.